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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/660,837	09/14/2000	Sunil Tomar	501	1616

2292 7590 12/15/2003

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EXAMINER	
ODLAND, DAVID E	

ART UNIT	PAPER NUMBER
2662	20

DATE MAILED: 12/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/660,837	TOMAR ET AL.	
	Examiner	Art Unit	
	David Odland	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-11,14,15,18,19,22,23 and 26-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-11,14,15,18,19,22,23 and 26-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4)☐ Interview Summary (PTO-413) Paper No(s). _____.
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other:

DETAILED ACTION

Response to Amendment

1. The following is a response to the amendments filed on 09/02/2003.

Claim Objections

2. Claim 1 is objected to because of the following informalities: Claim 1 recites that the receiving circuit receives bits over 'output' lines (in line 5). It appears as though this should recite that the receive circuit receive the bits over –input- lines, since it does not make sensed to receive data over output lines. The claim also recites sending the converted serial signals 'to one or more corresponding transmission circuit' in lines 10 and 11. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4,7-11,14,15,18,19,22,23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baylock (USPN 4,924,464), hereafter referred to as Baylock in view of Upp et al. (USPN 5,040,170), hereafter referred to as Upp.

Referring to claims 1,11,15,19 and 23, Baylock discloses an apparatus comprising:

a plurality of transmission circuits to transmit data over one or more of a set of output lines (a plurality of outputs that transmit data over output lines (see claim 1 and figure 6));

a plurality of receiving circuits to receive bits over one or more of a set of input lines (a plurality of inputs that receive data over the input lines (see claim 1 and figure 6)); and

a plurality of parallel-serial conversion circuits coupled to the plurality of transmission circuits and to the plurality of receiving circuits (a plurality of parallel-serial conversion coupled to the outputs and inputs (see claim 1 and figure 6)), the plurality of conversion circuits operable to convert a parallel signal to multiple serial signals including the received bits and send the converted serial signals to one or more corresponding transmission circuits (parallel signals are converted into serial signal by the converters and the converted signals are transmitted through the outputs (see claim 1 and figure 6)) and receive one or more sets of serial signals from one or more of the receiving circuits and convert the serial signals to parallel signals (serial signals are received and converted to parallel signals by the converters (see claim 1 and figure 6));

wherein stuffing data is added to the received bits in the multiple serial signals (the converters perform bit stuffing (see column 5 line 63 through column 6 lines 28)), at least one of the plurality of parallel-serial conversion circuits receives data at a first bit rate as a parallel signal (the converters receive parallel data at a particular rate (see claim 1 and figure 6)) and converts the parallel signals to multiple serial signals at a second bit rate (the parallel data is converted to multiple serial signals at a particular rate (see claims 1 and 6 and figure 6)), where the first bit rate is different than the second bit rate (the output clock rate is different that the input rate (see figure 6)), and the corresponding transmission circuit transmits the multiple serial

signals at the second bit rate (the converted multiple serial signals are output at the output clock rate (see claim 6 and figure 6)).

Baylock does not disclose that the number of multiple serial signals multiplied by the second bit rate is equal to the first bit rate. However, Upp discloses a system wherein bit stuffing is performed in the creation of SONET signals (see column 7 line 61 through column 8 line 6 and column 23 lines 25-52 and figure 10) such that parallel STS-3 SONET signal is converted to multiple serial SONET STS-1 signals, wherein the a STS-3 is 3 times an STS-1 (see column 6 lines 38-46 and figure 1). It would have been obvious to one skilled in the art at the time of the invention to implement this feature in the system of Baylock because doing so would allow proper timing and synchronization of the system.

Baylock also does not disclose that the parallel signal is SONET/SDH framed data. However, SONET Upp discloses a system for transporting SONET/SDH data frames (see abstract). SONET is a fast and an electro-magnetic (EM) interference resistant communications protocol because it uses light instead of electricity to transport data. Therefore, it would have been obvious to one skilled in the art at the time of the invention to implement the Baylock system using SONET/SDH because such a system would make Baylock faster and more reliable.

Note, regarding claims 15 and 23, Baylock discloses that the system performs both parallel to serial and serial to parallel conversions (i.e. both directions) (see figure 6)).

Referring to claim 2, Baylock discloses the system discussed above. Furthermore, Baylock discloses that a control circuit is coupled to the plurality of transmission circuits, to the plurality of receiving circuits and to the plurality of parallel-serial conversion circuits (a control signals, inherently from a controller, are sent to the output circuits, input circuits and conversion

circuits to control such elements of the system (see column 4 lines 9-29 and claim 1 and figure 6)), the control circuit to control conversion of signals between parallel and serial formats and to control transmission and receiving of data (the control signals are used to control the receptions, transmissions and conversions of the data (see column 4 lines 9-29 and claim 1 and figure 6)).

Referring to claim 3, Baylock discloses the system discussed above. Furthermore, Baylock discloses converting a received parallel signal to a corresponding serial signal at a first bit rate (the parallel-serial converter converts the parallel data into serial data at a particular rate (see claim 1 and figure 6)).

Referring to claim 4, Baylock discloses the system discussed above. Furthermore, Baylock discloses that one of the plurality of transmission circuits transmits the converted serial signal at the first bit rate (the parallel-serial converters transmit the converted signals at a particular rate (see claim 1 and figure 6)).

Referring to claim 7, Baylock discloses the system discussed above. Furthermore, Baylock discloses that one of the plurality of parallel-serial conversion circuits receives a serial signal at a first bit rate (the conversion circuit receives a serial signal at a first particular rate (see claim 1 and figure 6)) and converts the serial signal to a parallel data at the first data rate (the received data is converted into parallel data at the particular rate (see claim 1 and figure 6)).

Referring to claim 8, Baylock discloses the system discussed above. Furthermore, Baylock discloses that one of the plurality of receiving circuits receives the serial signal at the first bit rate and sends the serial signal to the parallel serial conversion circuit (the serial data is received at a particular rate and send to the serial-parallel conversion circuit to be converted (see claim1 and figure 6)).

Referring to claim 9, Baylock discloses the system discussed above. Furthermore, Baylock discloses that one of the plurality of parallel-serial conversion circuits receives multiple serial signals at a first bit rate (the conversion circuit receives multiple serial signals at a first particular rate (see claim 1 and figure 6)) and converts the serial signals to parallel data at a second bit rate (the serial signals are converted at a second particular rate (see claim 1 and figure 6)), where the second data rate is greater than the first bit rate (transmitting the parallel signal at a second rate which can be greater than the first particular rate (see claim 1 and claim 6)).

Referring to claim 10, Baylock discloses the system discussed above. Furthermore, Baylock discloses that one of the receive circuits receives the multiple serial signals at the first bit rate (multiple inputs circuits receive serial data at a particular rate (see claim 1 and figure 6)).

Referring to claims 14,18,22 and 26, Baylock discloses the system discussed above. Furthermore, Baylock discloses transmitting the multiple serial signals at the second bit rate using both a first transmitting circuit and a second transmitting circuit (data from the serial outputs are transmitted at a particular rate by way of a number of transmission circuits, including at least a first and second transmitting circuit (see claim 1 and figure 6)).

5. Claims 27-31are rejected under 35 U.S.C. 103(a) as being unpatentable over Baylock in view of Upp and further in view of Flanagan et al. (USPN 5,159,595), hereafter referred to as Flanagan.

Referring to claims 27-31, Baylock discloses the system discussed above. Furthermore, Baylock discloses that the number of serial signals is four (see figure 6)). Baylock does not disclose that the first rate corresponds to an STS-48 signal and the second rate corresponds to an

STS-12 signal. However, Flanagan discloses of a SONET system wherein the system communications STS-48 signals that are made up of four STS-12 signals (see column 7 line 53 through column 8 line 8)). It would have been obvious to one skilled in the art at the time of the invention to implement this SONET configuration in Baylock because SONET and in particular STS-48 is a fast (even faster than STS-3, as taught in Upp) and an electro-magnetic (EM) interference resistant communications protocol because it uses light instead of electricity to transport data. Therefore, it would have been obvious to one skilled in the art at the time of the invention to implement the Baylock system using SONET/SDH because such a system would make Baylock faster and more reliable.

Response to Arguments

6. Applicant's arguments filed 09/02/2003 have been fully considered but they are not persuasive.

On page 11 paragraph 2 and page 12 paragraph 2, the Applicant contends that "...Upp fails to disclose adding stuffing data (e.g., zeros or other "dummy" bits)..." and "Although Upp describes this insertion as "stuffing" the DS-3 formatted data into a SONET format, UPP fails to disclose actually adding any type of stuffing data..." The Examiner respectfully disagrees. Firstly, none of the claims recite that the stuffing data includes 'zeros or other "dummy" bits'. Secondly, assuming *arguendo*, and the claims did recite such limitations, Upp does indeed disclose that the zeros and other bits are stuffed into the SONET frame (see column 23 lines 25-52). Lastly, Baylock discloses that a bit stuffing procedure is used in the serial/parallel conversion processes (see column 5 line 63 through column 6 line 28).

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Odland, who can be reached at (703) 305-3231 on Monday – Friday during the hours of 8am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou, can be reached at (703) 305-4744. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, who can be reached at (703) 305-4750.

deo

December 2, 2003

HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
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